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Complete Instruction Set Summary 4.1 Instruction Set
Summary Mnemonics Operands Description Operation
Flags #Clocks #Clocks XMEGA Arithmetic And Logic
Instructions ADD Rd, Rr Add Without Carry Rd ← Rd +
Rr Z,C,N,V,S,H 1 ADC Rd, Rr Add With Carry Rd ← Rd +
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8127FS-AVR-02/2013 4. Register Summary Note: 1. For Compatibility With Future Devices, Reserved Bits Should Be Written To Zero If Accessed. Reserved I/O Memory Addresses Address Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Page 0x3F SREG I T H S V N Z C Page 12 0x3E SPH Stack Poin Mar 8th, 2024

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Instruction Set Manual 0856J-AVR-07/2014 4 2.3 I/O Direct Figure 2-3. I/O Direct Addressing Operand Address Is Contained In Six Bits Of The Instruction Word. N Is The Destination Or Source Register Address. Note: Some Complex AVR Microcontrollers Have More Peripheral Units Than Can Be ... Jun 4th, 2024

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16M-BIT [x 1 / X 2] CMOS SERIAL FLASH 32M-BIT [x 1 / X 2 ...

The MX25L1605D Are 16,777,216 Bit Serial Flash Memory, Which Is Configured As 2,097,152 X 8 Internally. When It Is In Two I/O Read Mode, The Structure Becomes 8,388,608 Bits X 2. The MX25L3205D Are 33,554,432 Bit Serial Flash Memory, Which Is Configured As 4,194,304 X 8 Internally. When It Is In Two I/O Read Mode, The Structure Be- Feb 7th, 2024

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