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2 / 15 Dynamic Gates Operate In Two Phases:  
Precharge And Evaluation. During The Precharge  
Phase, The Clock Is Low, Turning On The PMOS Device  
And Pulling The Output High. During Evaluation, The  
Clock Is High, Turning Off The PMOS Device. The  
Output May "evaluate" Low Through The NMOS  
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Nd.edu Assume Want To Shift Left By  $K$ ,  $0 \leq K \leq N-1$  ( $N = 2^n$ )  $K$  Expressible As  $N$ -bit Number:  $-K = K_{n-1}2^{n-1} + K_{n-2}2^{n-2} + \dots + K_12^1 + K_0$ ,  $K_i \in \{0, 1\}$  Barrel Shifter: Construct From  $N$  Levels Of  $N/2$ -in Multiplexors - When Level  $i$  Either Shifts Last Level By  $2^{i-1}$  Or Pass Unchanged Circuits-C Sli 2th, 2024 Introduction To CMOS VLSI Design Circuits-A CMOS VLSI Design Slide 2 Outline: Circuits Lecture A - Physics 101 - Semiconductors For Dummies - CMOS Transistors For Logic Designers Lecture B - NMOS Logic - CMOS Inverter And NAND Gate Operation - CMOS Gate Design - Adders - Multipliers Lecture C - P 26th, 2024. Introduction To CMOS VLSI Design (E158) Harris Syllabus ... MIPS Assembly Language From Chapter 3, ALU Design From Chapter 4, And The Multicycle Processor ... Labs And Problem Sets Are Due By The End Of Class And Will Not Be Graded If Submitted Late Because Solutions Will Be Given Out. However, The Labs Build Toward Assembly Of The Entire Processor In Lab 5, So It 26th, 2024

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