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- Configuration Design Security In Intel MAX 10 FPGA. Overview Of The Design Security Feature. The Design Security Feature For Intel FPGAs Protects Against Unauthorized Copying , Reverse Engineer Feb 7th, 2024.

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Introductory Paragraph In About This Guide. Changed "100 MHz" To "10 MHz" In Third Paragraph, Updated Fourth Paragraph, And Added "GTP" And UG482 May

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