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Will Release The Local Bus During T4 Of The Cycle When All The Following Conditions Are Met: 1.Request Occurs On Or Before T2. 2.Current Cycle Is Not The Low Byte Of A Word (on An Odd Address). 3.Current Cycle Is Not The First Acknowledge Of An Interrupt Acknowledge Sequence. 4.A Locked Instruction Is Not Currently Executing. 1th, 2024

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TowARD Thè End Of Anchises' Speech In Thè Sixth ...

Excudent Alii Spirantia Mollius Aera (credo Equidem),

Uiuos Ducent De Marmore Uultus, Orabunt Causas

Melius, Caelique Meatus Describent Radio Et Surgentia

Sidera Dicent : Tu Regere Imperio Populos, Romane,

Mémento (hae Tibi Erunt Artes), Pacique Imponere 3th,

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•Write Line Indicates 8086/8088 Is Outputting Data To A Memory Or I/O Device. -during The Time WR Is A Logic 0, The Data Bus Contains Valid Data For Memory

Or I/O -high-impedance During A Hold Acknowledge
INTA •The Interrupt Acknowledge Signal Is A Response
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