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Product Change Notification - SYST-17GQNW059

2) Section 2.7 Oscillator Value Conditions On Device Start-up A) Corrects The Oscillator Source Frequency.
3) Section 3.0 CPU A) Changes To Note 1 Here And Every Chapter Throughout Document. 4) Section 4.0 Memory Organization A) Changes To Figure 4-11 And Figure 4-16. B) Changes To Table 4- 1th, 2024

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DS20005397E-page 6 2015-2019 Microchip Technology Inc. 3.0 MEMORY ORGANIZATION The SST25PF040C SuperFlash Memory Arrays Are Organized In 128 Uniform 4 KByte Sectors, With 8 64KByte Overlay Erasable Blocks. FIGURE 3-1:

MEMORY MAP 4.0 DEVICE OPERATION SST25PF040C Is Accessed Through The SPI 1th, 2024

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ATSAMA5D27-SOM1-EVAL ATSAMA5D27-SOM1
24AA025E64T-I/SN 24AA025E64T-I/OT 24AA025E64T-E/SN 24AA025E64T-E/OT 24AA025E64-I/SN
24AA025E64-E/SN SYST-01LWMO536 - Data Sheet - 24AA02EXX/24AA025EXX/2K I2C Serial EEPROMs With EU1-48 Or EU1-64 Node Identity Date: Saturday, March 03, 2018 4th, 2024

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