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[1] Kashyap K. Patel, Nilesh D. Patel, " Phase Frequency Detector And Charge Pump For DPLL Using 0.18µm CMOS Technology" International Journal Of Emerging Technology And Advanced Engineering , ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3 Issue1, Page No. 55-58, January 2013) Mar 14th, 2024

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Controlled By The Setting Of Switches 3 A Nd 4 On The Front Edge Of The Detector. S Om Eti M Es When B Uried Loops A Re In Close P Ro Xim Ity To E Ach Other , It Ma Y Be Necess A R Y To Select Different Frequencies For Ea Ch B Uried Loop To A Void Loop Interfe Rence (Co Mmonly C Alled Crosstalk). The Actual Loop Operating Apr 10th, 2024

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