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Bare Meta/Linux Documentation Is Available In Appendix C: Zynq UltraScale+ RFSoC RF Data Converter Bare-metal/ Linux Driver. 3. For The Supported Versions Of Third-party Tools, See The Xilinx Design Tools: Release Notes Guide. Chapter 1: IP Facts PG269 (v2.3) June 3, 2020 Www.xilinx.com Zynq UltraScale+ RFSoC RF Data Converter 6. Se N D Fe E D ... 4th, 2024

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Getting Started With OpenCL On The ZYNQ Version: 0:5 Base Address, See Section 3.3. The Directly Important Pieces Of Information Here Is The Control Register, The Group Id Registers And The A,b And C Data Registers. Control: Using This Register We Can Start Computations In The Vadd Hardware Unit And Also Poll For The Done Signal. 2th, 2024

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